formed within the base region **21***j* in close proximity to the outer lateral border of the base region **21***j* so as to minimize the "L" dimension of the intrinsic FET **42** portions of the composite device. It will be appreciated from a review of FIG. **13**, that the critical "L" dimension for the intrinsic FET **42** extends along the entire length of the serpentine emitter region, and that by extending the emitter region in such serpentine-like fashion, the active channel portion of the intrinsic FET **42** can be significantly increased. The particular cross sectional configuration of the channel-collector transistor **20***j* selected in FIG. **14** resembles that configuration for the **20***f* channel-collector transistor previously disclosed in FIG. **9**, which employs the "J process". It will be recalled that use of the "J process" in the channel-collector transistor configuration eliminates the emitter-push layer deformation in the active channel region of the device, thus minimizing the current-limiting effect of the intervening FET portions **41** of the device.

Referring to FIGS. **13** and **14**, it will be observed that the collector region **23***j* and the base region **21***j* have been "interdigitated". Besides providing higher current handling capability and improved operating performance characteristics, the combination of the interdigitated base and collector regions and the serpentine emitter configuration, makes the channel-collector transistor with these properties highly attractive for use within integrated circuit networks since all of the output terminals of the composite device (i.e. the collector region **26**, the base region **21** and the emitter region **22**) are accessible to integrated circuit metallization paths without requiring a cross-over of metallization paths (i.e. multi-layer metallization layers are not required) to gain electrical access to the respective output ports of the device. It will be appreciated that all of the device configurations illustrated in the Drawing can be incorporated in both the serpentine emitter and the interdigitated collector-base configurations, similar in manner to that illustrated in FIGS. **13** and **14**.

Throughout the Drawing, the device geometries and relative dimensions of various layers and regions thereof have been grossly misproportioned in an effort to simplify definition of the various device configuration. A more accurate scaled diagram of a portion of that configuration of a channel-collector transistor **20** which is disclosed in FIG. **2** is illustrated in FIG. **17**. A review of FIG. **17** for the relative dimensions and spacings of the respective layers and regions of the channel-collector transistor **20** will provide one with an appreciation of the "thinness" of the channel-collector area which provides the "merged" properties of the device. FIG. **17** also provides one with an appreciation for the effects of "emitter-push" on the collector-channel region thickness and with an awareness of the processing and design factors involved in decreasing the "L" dimension of the channel portion of either the intervening FET **41** or the intrinsic FET **42**.

Other modification of the invention will be apparent to those skilled in the art in light of the foregoing description. This description is intended to provide concrete examples of individual embodiments clearly disclosing the present invention. Accordingly, the invention is not limited to any particular embodiment, and various combinations of the processes and topological configurations of the solid state electronics art are anticipated hereby. Alternatives, modifications and variations of the present invention which fall within the spirit and broad scope of the appended claims are covered.

What is claimed is:

1. An improved merged channel-collector transistor semiconductor device, comprising:

(a) a body of semiconductor material defining an upper surface and characterized by:

(i) a base region of a first conductivity type extending from said upper surface;

(ii) a collector region of a second conductivity type opposite to that of said first conductivity type, forming an operative junction with said base region and defining an effective lower collector boundary of said collector region, which underlies and is spaced apart from said base region;

(iii) an emitter region of said second conductivity type forming an operative junction with said base region, said emitter region lying within the lateral extent of said base region;

(iv) that said collector region which is located below substantially the entire said base region and interposed between said base-collector junction and said effective lower collector boundary being sufficiently thin and having controlled impurity concentration therethrough so as to cause said interposed collector region to simultaneously operatively function as an active collector region of a bipolar junction transistor and a channel region of a junction field-effect transistor, wherein the equivalent circuit of said channel-collector sharing field-effect and bipolar junction transistors approximates a cascode configuration;

(v) said emitter being configured such that at least one edge thereof, as viewed in top plan, lies in close proximity with a substantial portion of the periphery of said base region, for minimizing the lateral "L" dimension of that field-effect channel portion of said interposed collector region which comprises the outer peripheral portion thereof but which does not underlie said emitter region; and

(vi) wherein said emitter region is configured with at least one bend in serpentine-shape as viewed in top plan, for increasing the "W" dimension of that field-effect channel portion of said interposed collector region which comprises the outer peripheral portion thereof, but which does not underlie said emitter region; and

(b) means adjacent said effective lower collector boundary of said collector region for preventing majority carrier current flow from said collector region across said lower effective collector boundary.

2. An improved merged channel-collector transistor semiconductor device, comprising:

(a) a body of semiconductor material defining an upper surface and characterized by:

(i) a base region of a first conductivity type extending from said upper surface;

(ii) a collector region of a second conductivity type opposite to that of said first conductivity type, forming an operative junction with said base region and defining an effective lower collector boundary of said collector region, which underlies and is spaced apart from said base region;

(iii) an emitter region of said second conductivity type forming an operative junction with said base region, said emitter region lying within the lateral extent of said base region;